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PATENT & TRADEMARK OFFICE
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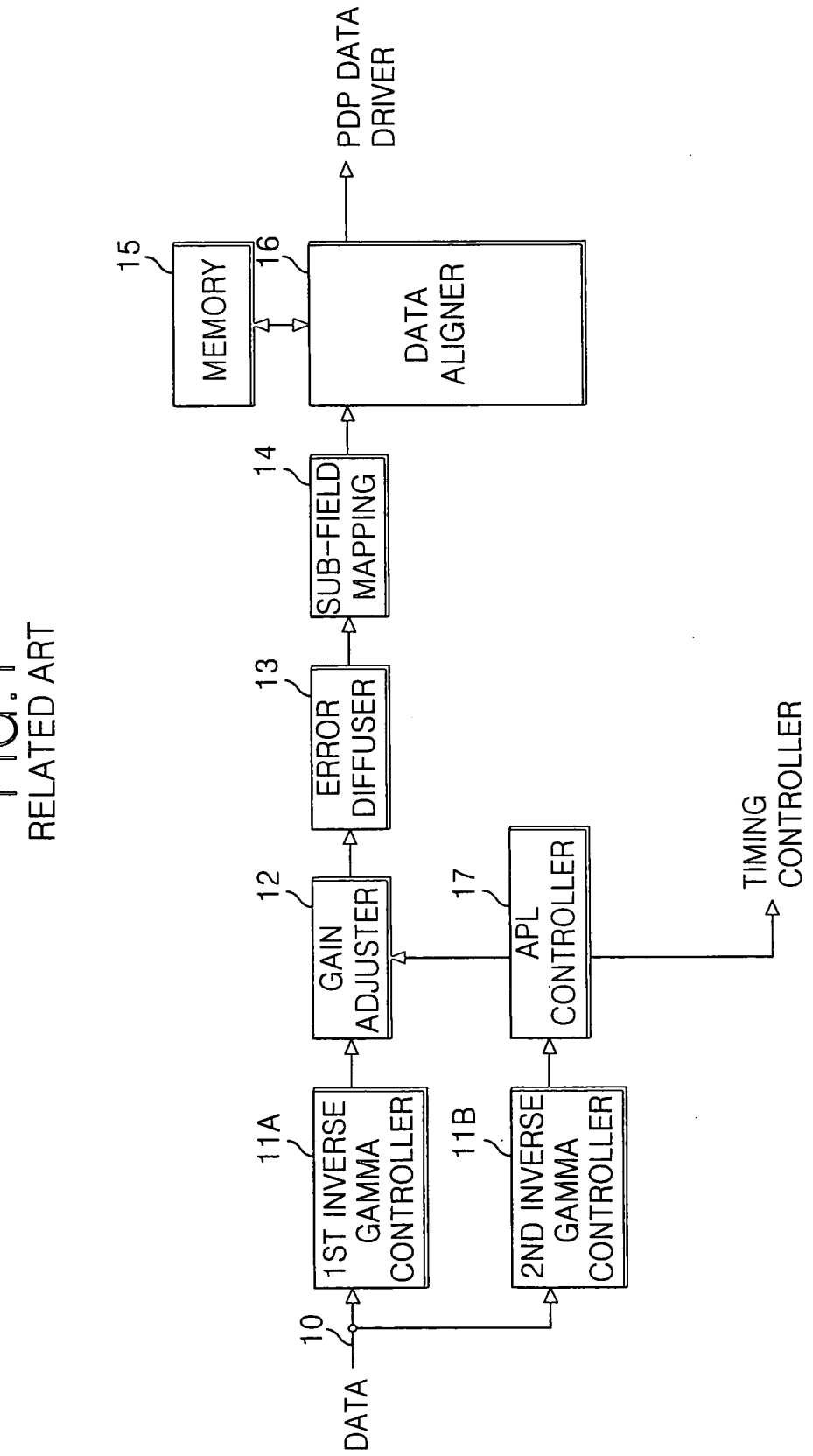


FIG. 1
RELATED ART

FIG.2

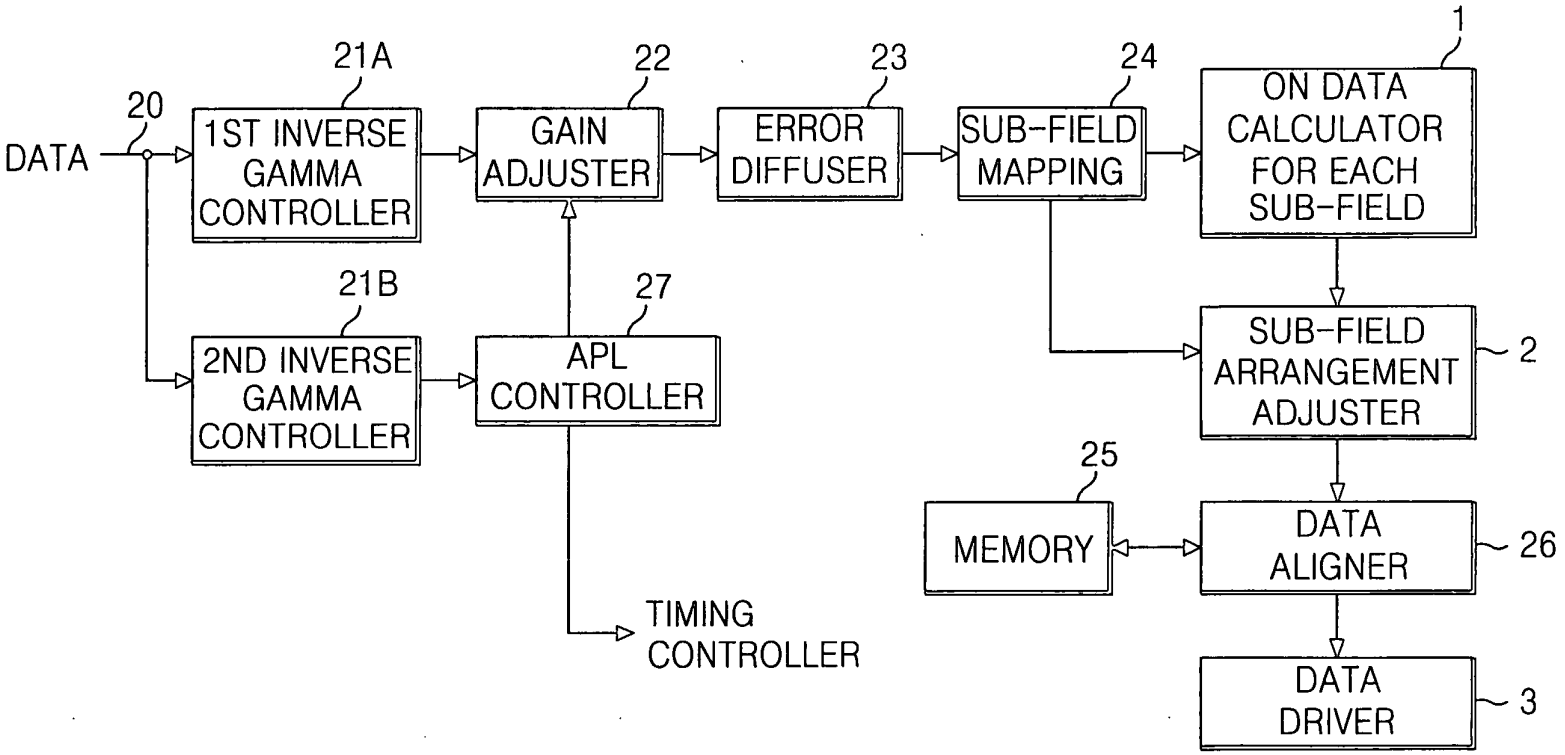

DATA
20
21A
1ST INVERSE GAMMA CONTROLLER
21B
2ND INVERSE GAMMA CONTROLLER
22
GAIN ADJUSTER
23
ERROR DIFFUSER
24
SUB-FIELD MAPPING
27
APL CONTROLLER
TIMING CONTROLLER
1
ON DATA CALCULATOR FOR EACH SUB-FIELD
SUB-FIELD ARRANGEMENT ADJUSTER
2
25
MEMORY
DATA ALIGNER
26
DATA DRIVER
3

FIG.3

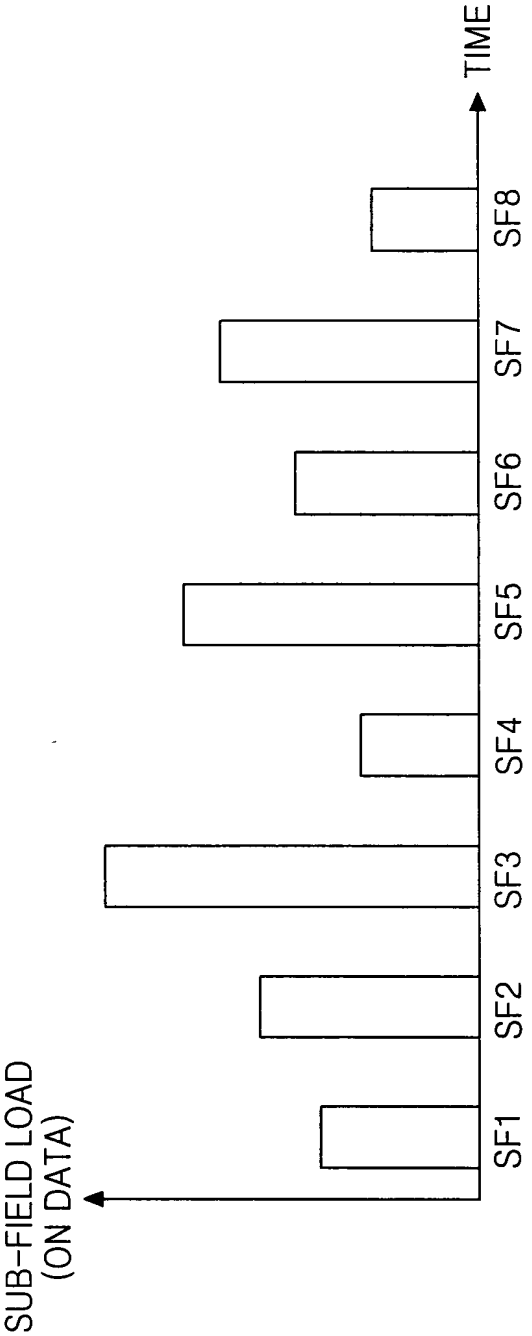


FIG.4

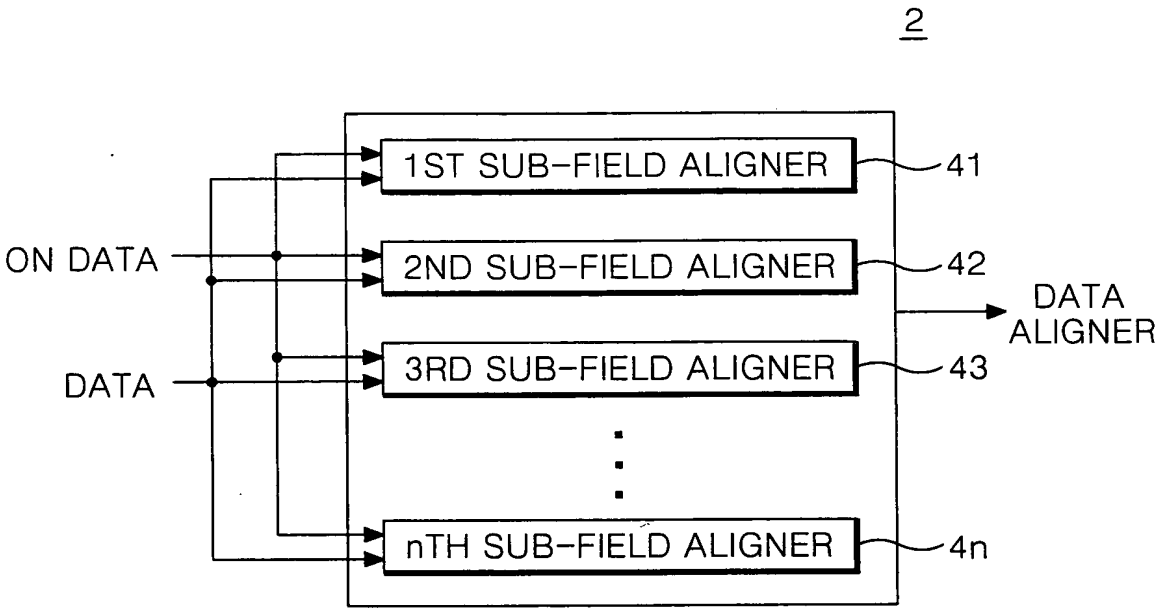

2
1ST SUB-FIELD ALIGNER
41
ON DATA
2ND SUB-FIELD ALIGNER
42
DATA ALIGNER
DATA
3RD SUB-FIELD ALIGNER
43
nTH SUB-FIELD ALIGNER
4n

FIG.5A

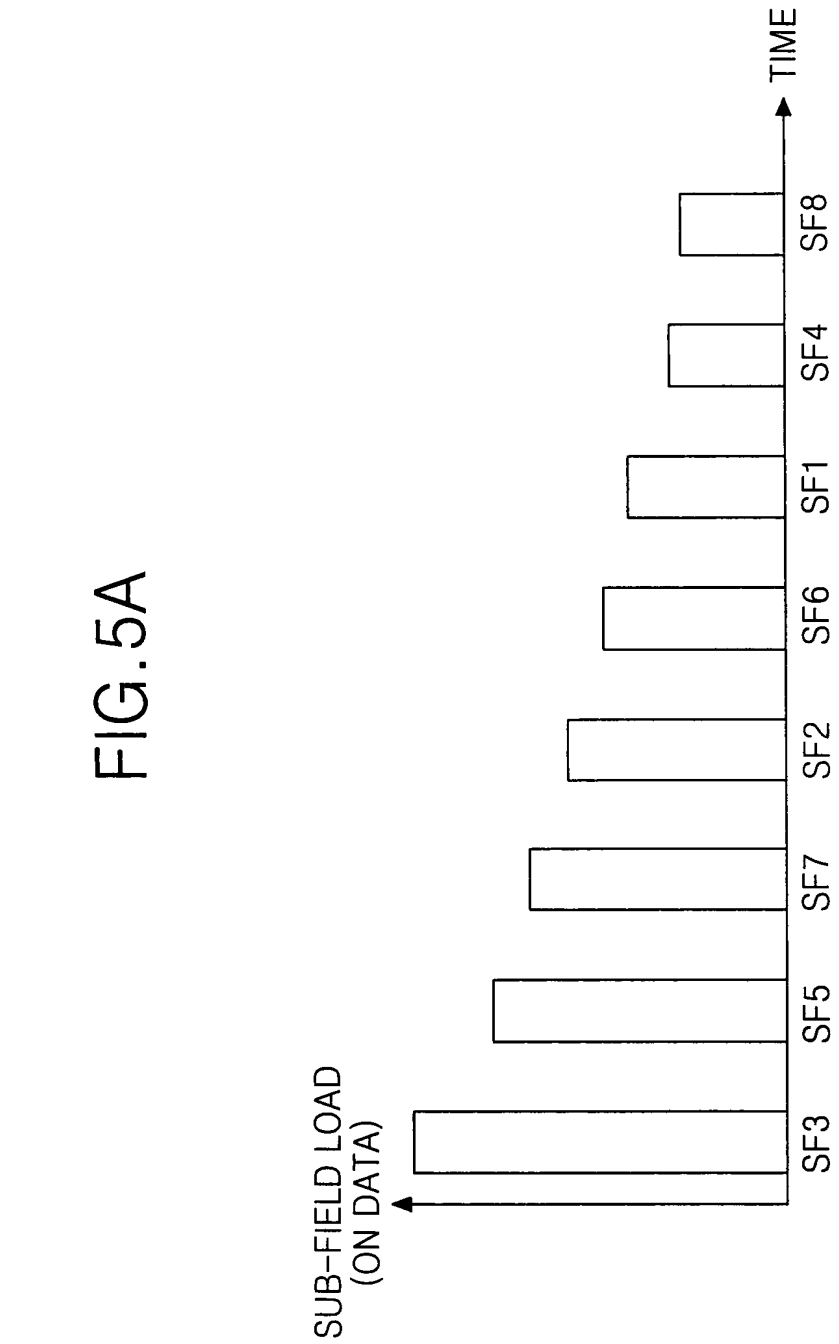


FIG.5B

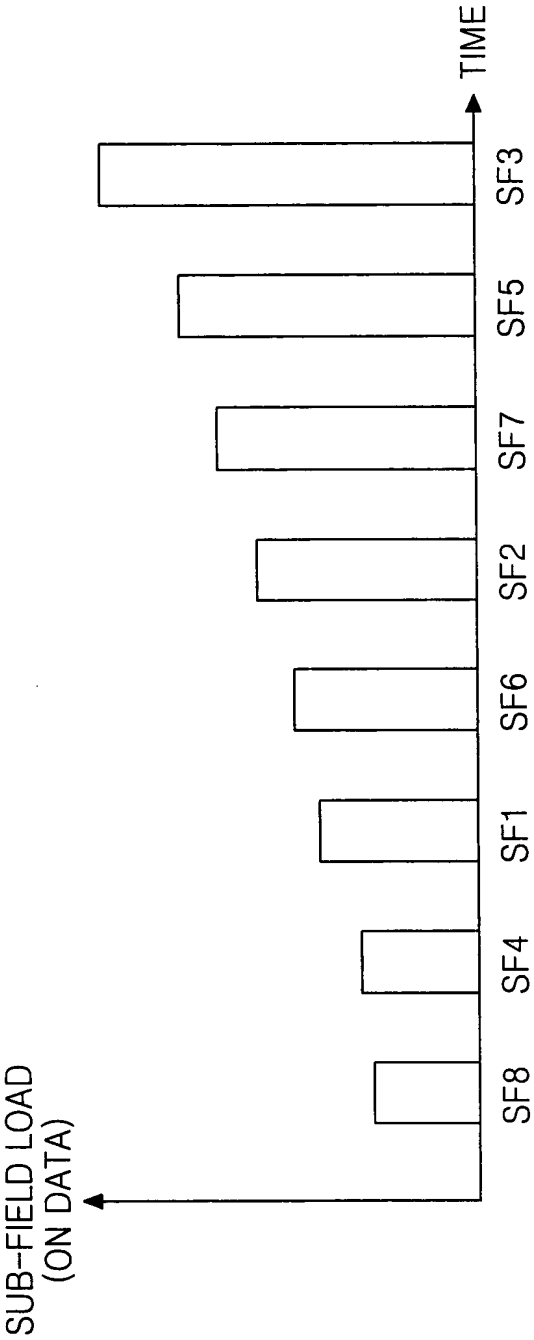


FIG.5C

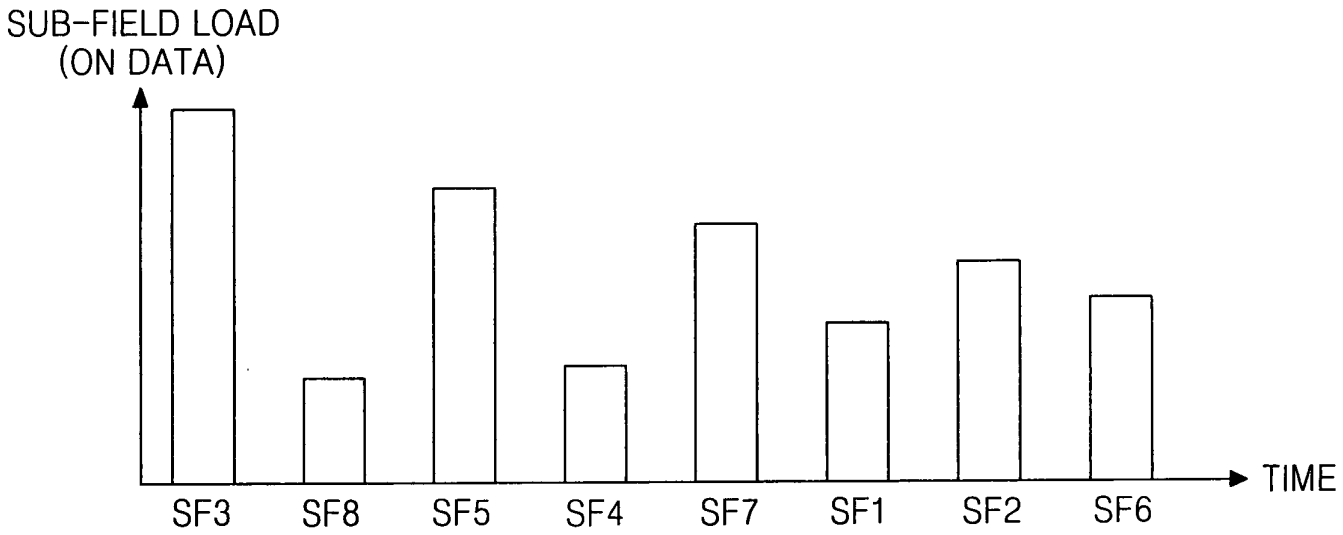


FIG.6

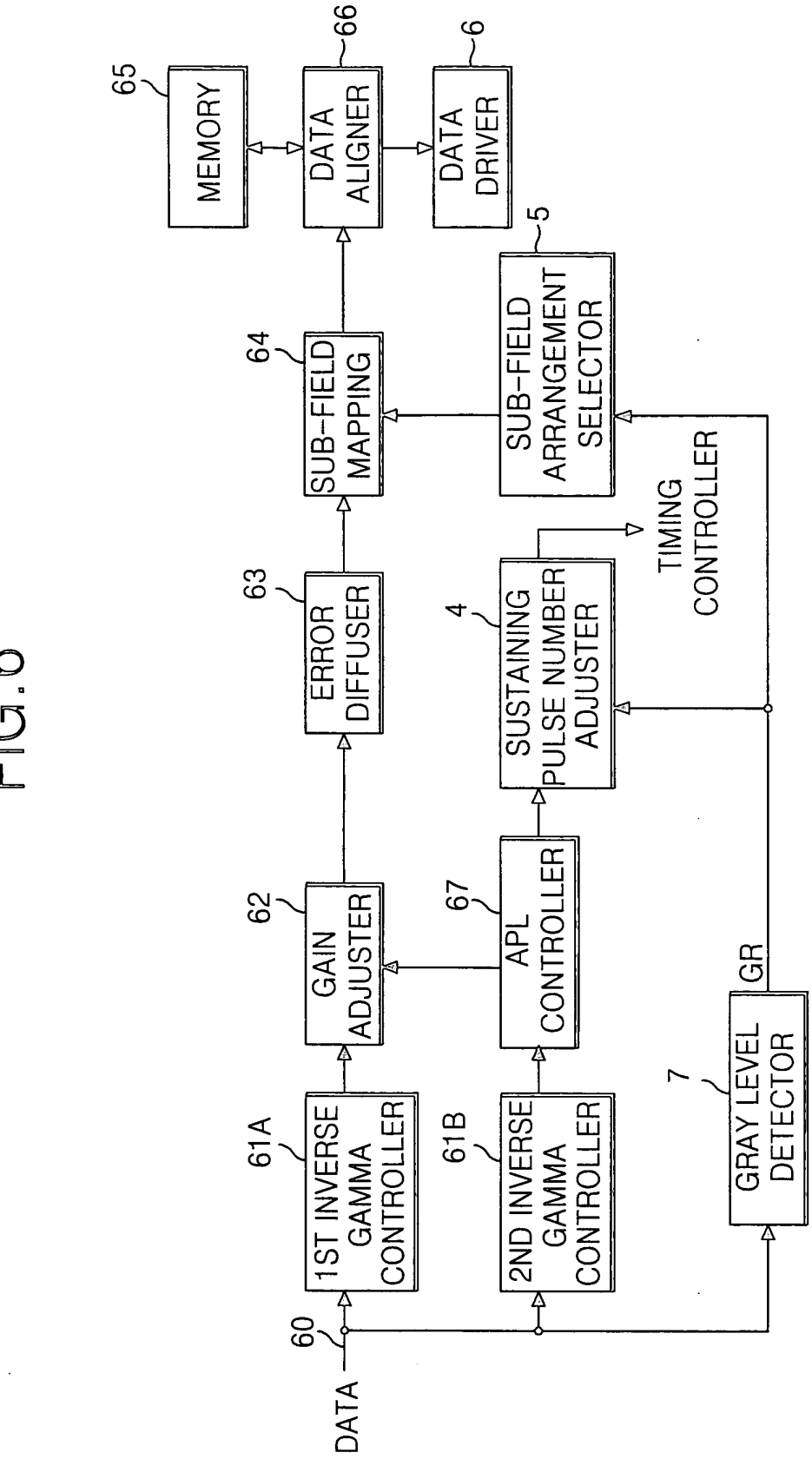

DATA
60
1ST INVERSE GAMMA CONTROLLER
61A
2ND INVERSE GAMMA CONTROLLER
61B
GAIN ADJUSTER
62
APL CONTROLLER
67
ERROR DIFFUSER
63
SUSTAINING PULSE NUMBER ADJUSTER
4
SUB-FIELD MAPPING
64
SUB-FIELD ARRANGEMENT SELECTOR
5
TIMING CONTROLLER
GRAY LEVEL DETECTOR
7
GR
MEMORY
65
DATA ALIGNER
66
DATA DRIVER
6

FIG.7A

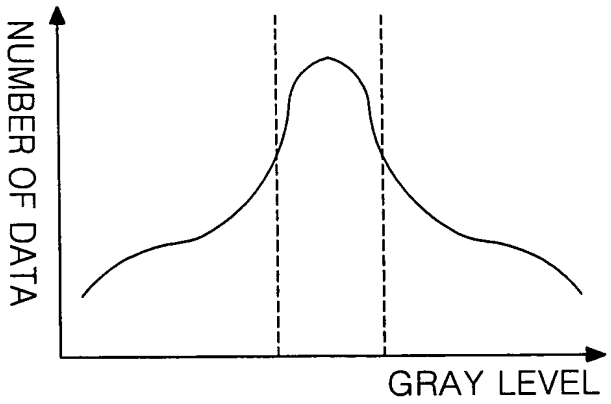


FIG.7B

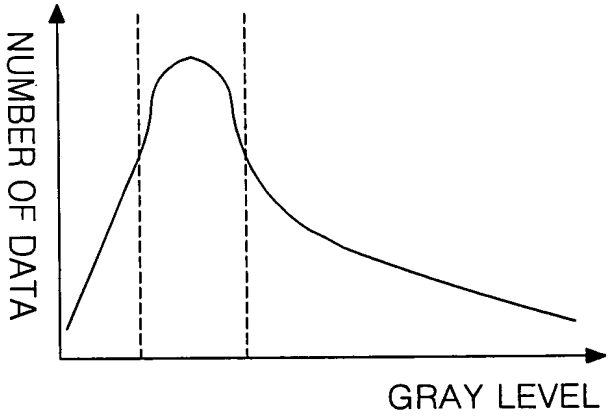


FIG.7C

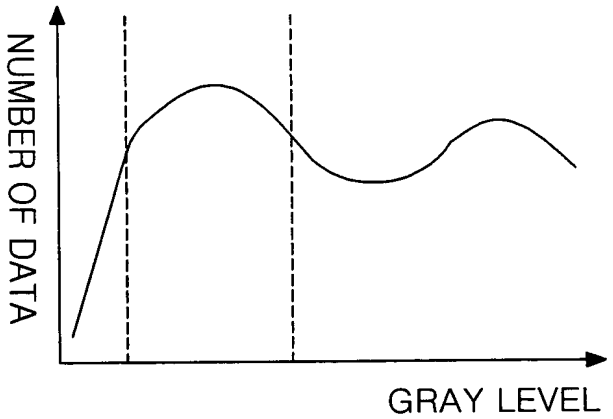


FIG.8

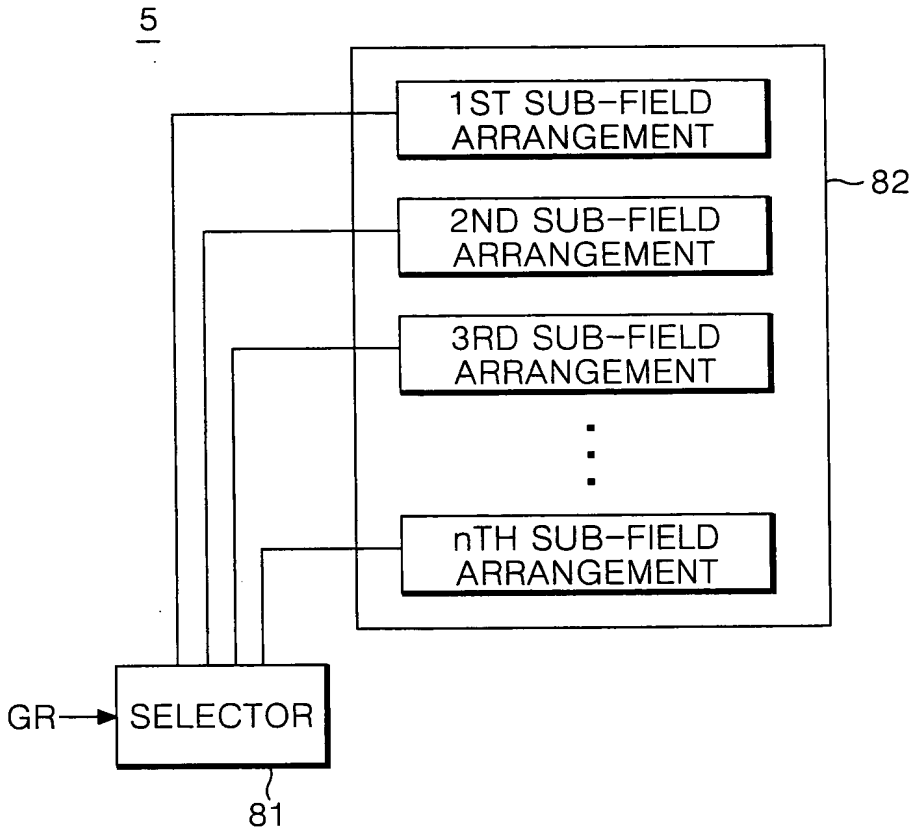
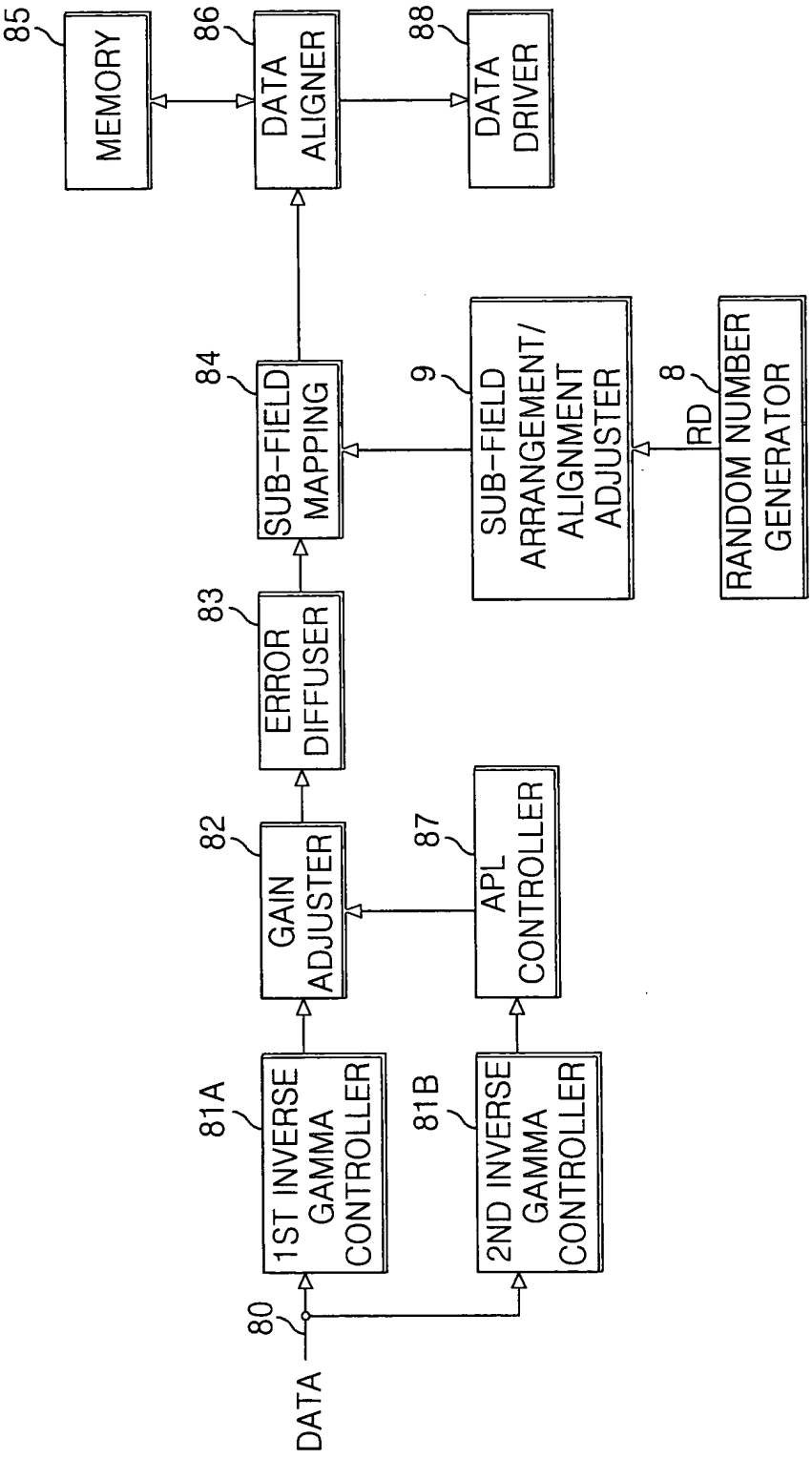

5
1ST SUB-FIELD ARRANGEMENT
2ND SUB-FIELD ARRANGEMENT
3RD SUB-FIELD ARRANGEMENT
nTH SUB-FIELD ARRANGEMENT
82
GR
SELECTOR
81

FIG.9


DATA
80
1ST INVERSE GAMMA CONTROLLER
81A
2ND INVERSE GAMMA CONTROLLER
81B
GAIN ADJUSTER
82
APL CONTROLLER
87
ERROR DIFFUSER
83
SUB-FIELD MAPPING
84
SUB-FIELD ARRANGEMENT/ ALIGNMENT ADJUSTER
9
RD
RANDOM NUMBER GENERATOR
8
MEMORY
85
DATA ALIGNER
86
DATA DRIVER
88